refBhavnagarwala05

Since SRAM failure statistics are strongly dependent on the operating voltages, the authors claim that playing with the cell voltages is an effective way to reduce read and write failures.

The write assist technique proposed is to raise the cell VSS which not only lowers the node voltage distribution when writing a 0, but also raises the trip-point of the inverter storing the 0. Thus, it becomes easier to flip the cell. This solution however is expensive in terms of power and retention margin of half-selected cells also needs to be considered. Layout complexity is also increased.

refShibata06

Another way of improving write margin is to strengthen the access transistor. This paper explores this option and proposes a negatively driven bitline that increases the drive strength of the access transistor. In addition, the authors propose using MTCMOS methods and SoI technology to get lower power dissipation for a given performance constraint.

A major limitation is that the proposed technique is verified in 0.35 μm technology, but variation effects in modern technologies can make this technique less effective.

refKawasumi08

Scaling increases variation and reduces noise margins. Ways to improve margins so that scaling can continue need to be explored, without having to resort to area expensive solutions such as 8T or power and complexity expensive solutions such as dual power supplies.

A single power-supply, unit β-ratio, 45nm 6T SRAM cell is proposed that can work down to 0.7V. The proposed cell allows us to optimize one side of the bitcell for write by making the access transistor the same size as the pulldown on one side (i.e strengthening it w.r.t the pull up when compared to a conventional symmetric 6T cell). In addition, the sizing scheme ensures that the cell layout is "notchless", thus mitigating the manufacturing variability effects due to Line Edge Roughness.

refPilo07

Yield loss at V_{DDmin} occurs due to write failures, read upsets, read signal failures and retention failures. This paper aims to provide circuit solutions to address the first three failure mechanisms.

By collapsing the cell supply, the pfet is weakened and makes the cell less stable and easier to write. However, lowering the cell supply too much can lead to retention related failures in the unaccessed or half-selected cells.

refBhavnagarwala08

This paper is a follow-up Journal paper on refBhavnagarwala08 and elaborates on the idea presented in refBhavnagarwala05. A few other additional cell-supply based write assist schemes are investigated and their impacts on cell writability (and read stability) are compared. The following techniques are explored

- Dual dynamic VDD
- Dual Static VDD
- Single static VDD with dynamic local VGND, low V_T PFET and sub VDD BL precharge

The authors claim that the third technique (local VGND raised during write) is the best write assist technique.

The paper suffers from the same limitations as refBhavnagarwala05